A 3.2 GHz, 26 dB Wide-Band Monolithic Matched GaAs MESFET Feedback Amplifier Using Cascodes

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Abstract—**Feedback around cascode stages is demonstrated to be a useful means of making matched direct coupled amplifiers with higher bandwidths than afforded by conventional common source topologies. Design techniques are described for an amplifier which is capable of operation to dc and which exhibits a measured gain of 26 dB, a 3.2 GHz bandwidth, and a 2.5:1 VSWR in a 1 μm GaAs MESFET process. A novel adjustment scheme is introduced whereby the amplifier's frequency response can be modified via a dc bias voltage to ensure stable circuit operation in spite of MESFET modeling inaccuracies and GaAs processing variations.**

I. INTRODUCTION

ADVANCED silicon and GaAs IC technologies have made possible monolithic direct coupled amplifiers with gigahertz bandwidths and with input/output ports matched to standard 50 Ω or 75 Ω impedances. The attainable gain–bandwidth products improve with smaller dimensions of the active devices. While several interesting design techniques have appeared in silicon bipolar [1], [2] and NMOS [3] technologies, most of the GaAs amplifiers in this genre [4]–[6] follow a topology that was introduced several years ago [7]. This type of design (Fig. 1) is well proven in its insensitivity to threshold voltage and other processing variations. Local shunt feedback is employed around a single common source stage, so that the magnitude of the gain is determined by the ratio of the input device gate width to the feedback device width, where all devices have the same gate length.

The attainable gain and bandwidth in such a scheme are limited by the fact that feedback is applied around only a single inverter. Intrinsically, a MESFET displays the maximum open-loop voltage gain when it drives an ideal current source as its load. For a 1 μm channel length MESFET, the maximum high-frequency gain is about 10, determined by the ratio of the transconductance (g_m) to the output conductance (g_d), and there is one dominant pole at the output node. Applying feedback around this stage produces a trade-off between gain and bandwidth. Cascading several such local feedback stages is a common means to enhance the gain, but always at the price of some bandwidth shrinkage. Thus, a previously announced two-stage amplifier [8] with a gain of 22 dB and a bandwidth of 2.5 GHz was regarded as attaining the limits of a 1 μm MESFET technology. A performance of 26 dB at 3.3 GHz for an amplifier in this technology was reported even earlier [9] with a common gate stage used to provide input matching [10]. This circuit, however, amounted to a cascade of three stages where the common gate input FET was followed by a traditional two-stage topology. Further, the output stage was not matched to 50 Ω, so the circuit obtained an additional 4.5 dB of gain over that of an output matched circuit. Also, the common gate gain stage at the input necessitated the use of on-chip coupling capacitors in the signal path, precluding dc operation.

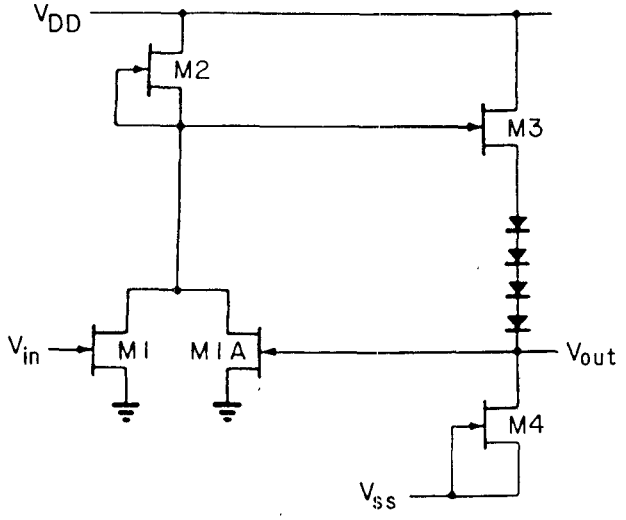

Fig. 1. The traditional shunt feedback topology in GaAs direct coupled amplifiers.

It is desirable in many applications to obtain higher gain *and* higher bandwidth than afforded by the schemes mentioned above. We describe an implementation which relies upon feedback around GaAs MESFET cascode stages [11], [12] to achieve this goal. Design techniques are presented for optimizing the gain–bandwidth product, for biasing

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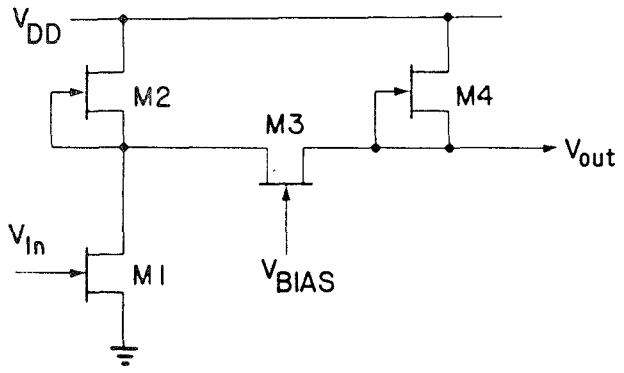


Fig. 2. A cascode stage in MESFET's.

the cascode on-chip, and for adjusting the frequency response via an external dc voltage to ensure stability.

II. Gain and Bandwidth of Cascodes

To overcome the limitations of previously reported topologies, feedback must be applied around a stage with a higher gain-bandwidth product. The gain–bandwidth product may be improved over a single inverter, in principle, by cascading two such inverters. For two stages with identical gain, G, and bandwidth, B, the gain–bandwidth product of the cascade is $G^2B\sqrt{2^{1/2}-1}$, a significant increase over that of one stage, GB. However, the cascade of two inverters is noninverting, so that simple resistor feedback applied around such an amplifier is regenerative. A cascade of three inverters offers a net inversion; however, a feedback loop here is potentially unstable because of the phase shift accumulated by a signal passing through these stages. Only under certain special conditions has this method been used successfully to design very broad band amplifiers [13], [14].

On the other hand, an inverting cascade of only *two* gain stages may be obtained by using the cascode configuration. The cascode (Fig. 2) consists of a common source stage (inverting), followed by a common gate stage (noninverting). The total gain (G_{casc}) of a FET cascode circuit is [15]

$$G_{\text{casc}} = -\frac{g_{m1}}{g_{d4}}\frac{g_{\text{in}}}{g_{\text{in}}+g_{d1}+g_{d2}} \tag{1}$$

where g_{in} is the conductance looking into the source of the common gate transistor, M3. This conductance may be determined by calculating the voltage swing, v_x, produced at the source of M3 when a test current i_x is injected into it with M1 and M2 disconnected. This procedure gives

$$i_x = g_{m3}v_x + g_{d3}(v_x - i_x/g_{d4}) \tag{2}$$

which, upon rearrangement, yields

$$\frac{1}{g_{\text{in}}} = \frac{v_x}{i_x} = \frac{1+g_{d3}/g_{d4}}{g_{m3}+g_{d3}} \approx \frac{1}{g_{m3}}(1+g_{d3}/g_{d4}). \tag{3}$$

Note that with large load impedances (small g_{d4}) this expression indicates that the common gate input impedance can be significantly greater than the usual approximation, $1/g_m$. Thus,

$$G_{\text{casc}} = -\frac{g_{m1}}{g_{d4}}\frac{1}{1+\left(\frac{g_{d1}+g_{d2}}{g_{m3}}\right)(1+g_{d3}/g_{d4})}. \tag{4}$$

G_{casc} is maximized when g_{d4} equals zero. In this case a gain almost equal to the product of the individual gains of two common source stages results because then

$$G_{\text{casc}}|_{g_{d4}=0} = -\frac{g_{m1}}{(g_{d1}+g_{d2})}\frac{g_{m3}}{g_{d3}}. \tag{5}$$

By choosing the gate width of M4 to be about 1/10th the combined widths of M1 and M2, g_{d4} is made quite small. In this manner, cascode gain stages can be designed with a significantly higher gain–bandwidth product than a comparable common source amplifier. The circuit described in this paper uses feedback around cascodes to demonstrate an input/output matched, wide-band amplifier with higher gain–bandwidth product than any previously reported circuits fabricated in a 1 μm technology.

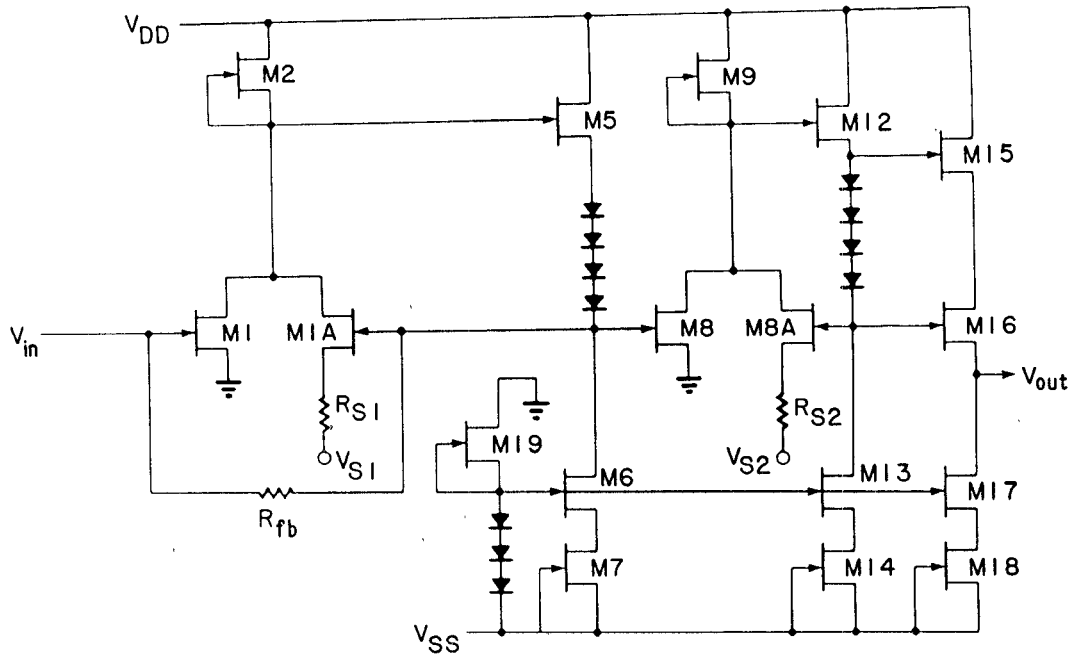
Another important advantage of the cascode configuration is that it demonstrates improved frequency response compared to the common source topology. This bandwidth improvement arises because the Miller multiplication of C_{gd1} decreases as g_{m3} increases. The three important poles of the cascode circuit are associated with time constants seen at the gate of M1, the drain of M1, and the drain of M3. By adjusting device geometries these pole frequencies can be made nearly equal to one another, thus eliminating dominant poles. The closed-loop poles will then be complex, and may, in theory, be adjusted to provide maximally flat response.

Because of modeling inaccuracies and process variations, reliable placement of the closed-loop poles in a high-frequency feedback amplifier is very difficult in practice. Since the poles in this amplifier must be complex to obtain maximum broad-banding, stability is a very important issue. If the amplifier is overdamped, the bandwidth is unduly narrow; but if the circuit is underdamped, excessive peaking or oscillations ensue. An important aspect of the amplifier design discussed here is a new compensation circuit which ensures stability while simultaneously allowing maximum bandwidth. This will be discussed in detail below.

III. Common Source Amplifiers

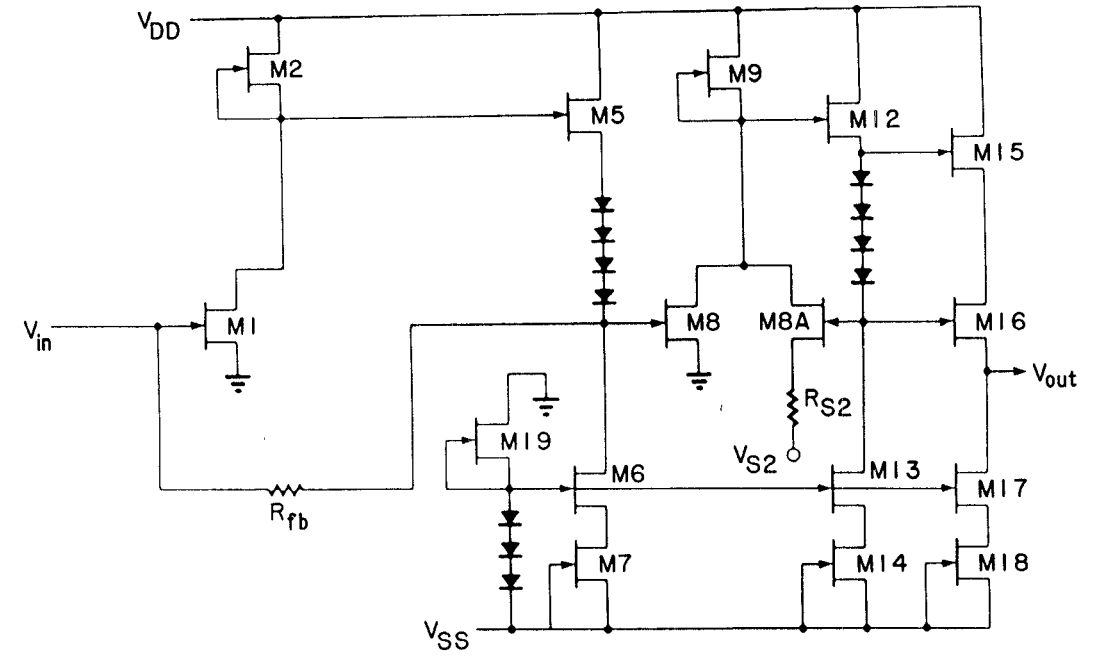
Before presenting the performance improvements made possible by cascodes, two variations on the standard topology [7] are first described. All of the amplifiers discussed below consist of two blocks: the first block is a transimpedance amplifier, providing a voltage gain with low noise and a matched input impedance; the second stage is used to enhance the gain further; finally, a voltage follower of appropriate size provides a matched output impedance.

Circuit CS-A (Fig. 3) is a cascade of two common source stages M1, M2 and M8, M9, with interstage buffer M5–M7 and output buffer M15–M18. Devices M1A and M8A provide local shunt feedback to obtain broad-banding of



R_{fb}	300 Ω
R_{s1}	250 Ω
R_{s2}	250 Ω
V_{s1}	−2 V
V_{s2}	−1 V
V_{DD}	+5 V
V_{SS}	−5 V
M1	500 μm
M1A	200 μm
M2	220 μm
M5	100 μm
M6	100 μm
M7	100 μm
M8	250 μm
M8A	100 μm
M9	110 μm
M12	100 μm
M13	100 μm
M14	100 μm
M15	150 μm
M16	150 μm
M17	150 μm
M18	150 μm
M19	10 μm

Fig. 3. Wide-band amplifier CS-A. Device sizes in inset.



R_{fb}	600 Ω
R_{s2}	250 Ω
V_{s2}	−1 V
V_{DD}	+5 V
V_{SS}	−5 V
M1	500 μm
M2	160 μm
M5	100 μm
M6	100 μm
M7	100 μm
M8	250 μm
M8A	100 μm
M9	110 μm
M12	100 μm
M13	100 μm
M14	100 μm
M15	150 μm
M16	150 μm
M17	150 μm
M18	150 μm
M19	10 μm

Fig. 4. Wide-band amplifier CS-B. Device sizes in inset.

the frequency response. This circuit is compared with an amplifier, CS-B (Fig. 4), that does not use the shunt feedback FET M1A. In circuit CS-B the value of R_{fb} has been adjusted to keep the input matched to 50 Ω. Both of these topologies were designed to obtain the maximum gain–bandwidth product, as simulated using SPICE and the circuit models described in a later section of this paper. A comparison of the frequency response of these two amplifiers (Fig. 5) shows that although the gain of CS-B is larger by 7 dB, the −3 dB bandwidth of CS-A is greater by 1.0 GHz due to the action of feedback FET M1A. In microwave applications, bandwidth is almost always at a greater premium than gain. Thus, CS-A is considered the better of the two common source circuits, exhibiting a gain of 15.3 dB with a bandwidth of 2.5 GHz.

We now describe a new circuit design that demonstrates 26 dB gain at a 3.2 GHz bandwidth.

IV. Cascode Circuit Design

Circuit CASC (Fig. 6) consists of the same two blocks as the previous circuits, but employs feedback around *cascode* stages to obtain broad-banding of the amplifier. Temporarily ignoring R_{fb} and C_{fb}, circuit operation can be analyzed as follows. Feedback current i_d (M1A) subtracts from i_d (M1), resulting in a small error current, i_e, flowing through transistors M2 and M3. If the feedback loop gain

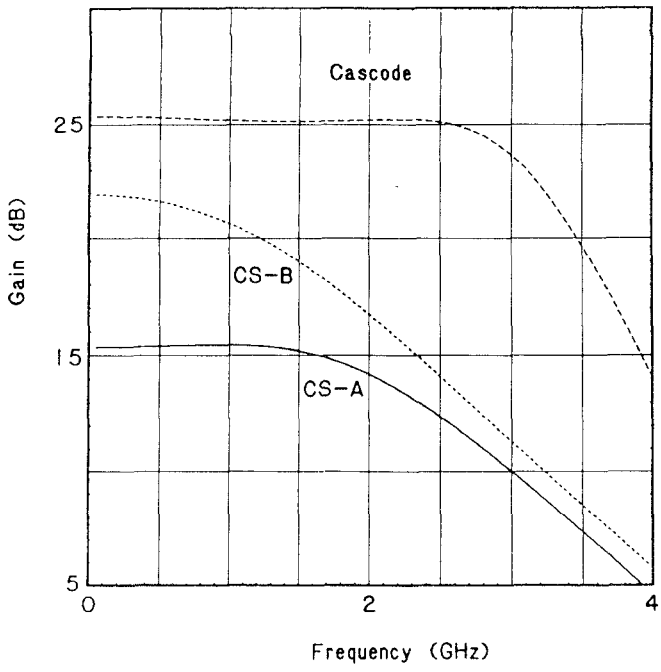


Fig. 5. Comparison of the simulated frequency response of amplifiers CS-A, CS-B, and CASC (whose circuit diagram appears in Fig. 6).

is large, i_e tends toward zero and KCL at the drain of M1 yields

$$g_{m1}V_{\text{in}} = -g_{m1a}V_{\text{out}} \tag{6}$$

or

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{g_{m1}}{g_{m1a}} \tag{7}$$

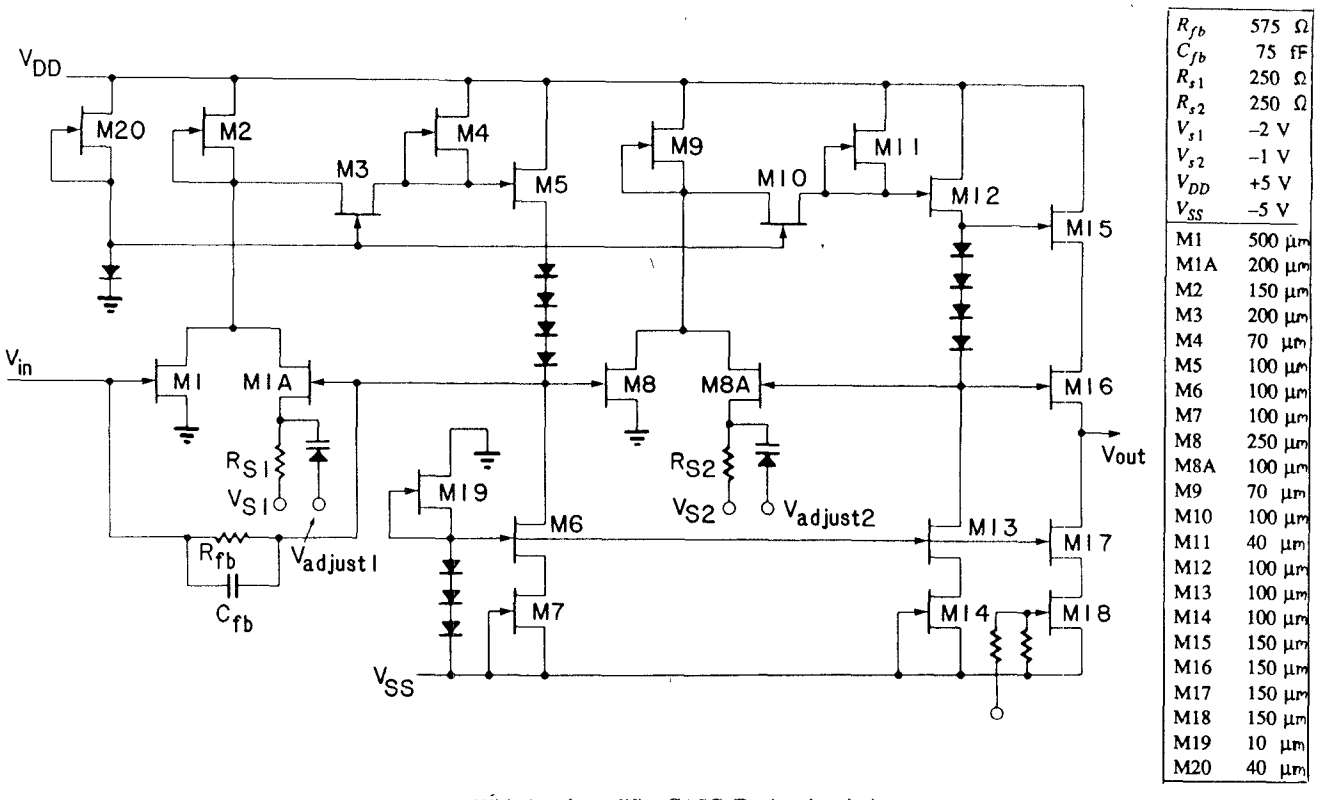
where the degenerative effect of R_{s1} has been neglected for simplicity. The bandwidth of the cascode feedback circuit is greatly improved over that of circuits CS-A and CS-B for two reasons. First, as mentioned previously, M3 reduces the impedance seen at the drain of M1, thereby reducing the Miller multiplication of C_{gd1}. Second, the loop gain of circuit CASC is much larger than in circuit CS-A; therefore, the broad-banding due to feedback is greater. In practice, the loop gain of circuit CASC can exceed the loop gain of circuit CS-A by over an order of magnitude. With R_{fb} included, the circuit changes from a voltage amplifier to a transimpedance amplifier which presents a 50 Ω input impedance to the driving source and which maintains the superior gain–bandwidth product of the cascode feedback topology.

Since a cascode circuit is essentially a two-stage inverting amplifier, a signal propagating through it experiences more phase delay than in a one-stage amplifier, and stability problems can arise when this topology is included within a feedback loop. To counteract the cumulative delay through the four FET's in each feedback loop, an $R-C$ network was introduced in the sources of the shunt feedback FET's. This network *controls the peaking* introduced at the band edge of the frequency response. The operation may be understood qualitatively by noting that at high frequencies, delays in the feedback loop cause i_d (M1A) to lag i_d (M1) in phase by more than the desired 180°. As this lag approaches 360°, excessive peaking appears in the frequency response and instability can result. This effect may be counteracted at the high frequencies where peaking appears by choosing the time constant of the $R-C$ network properly, because the feedback current may then be approximated by i_d (M1A) $\approx j\omega C v_g$ (M1A) and thus leads v_g (M1A) in phase by 90°, partially canceling the phase lag due to the delay accumulated through the amplifier. The capacitors may be implemented as reverse biased Schottky diodes to allow varactor-type control of the $R-C$ time constant with an off-chip dc voltage. By varying this dc voltage, the frequency response of the amplifier can be adjusted until an acceptable peaking is observed at the band edge. This method guarantees stability while allowing adjustment for maximum achievable bandwidth. It is worth noting that although the $R-C$ circuit resembles traditional shunt peaking, its effect in this application is quite different, serving more as a stability circuit. An alternate description of this effect is to note that the $R-C$ network adds a zero to the feedback function. This feedback zero affects the root locus by drawing the complex closed-loop poles away from the $j\omega$ axis. Varying the value of C changes the position of this feedback zero, which in turn alters the root locus and the amount of peaking in the frequency response. Since this procedure only perturbs slightly the poles near the band edge, the roll-off remains unaffected and the bandwidth changes by a negligible amount.

One concern in the design of cascode amplifiers is to provide a convenient means of biasing the gates of the common gate stages (M3 in Fig. 2). For depletion FET's, a natural way of doing this on-chip [16] is to bias the gates at the positive turn-on voltage of a Schottky diode (about 600 mV), and choose the current density in the common gate FET's so that they operate at a negative V_{gs}. With the feedback loop closed, the voltage at the drain of the common source FET (M1 in Fig. 2) can then be sufficiently positive to ensure that it operates in the saturation region of its $I-V$ characteristics. In this implementation, an important precaution is to provide adequate capacitive decoupling at the gate terminal of M3, because at high frequencies any resistance at the gate of M3 appears as an effective inductance at its source. This decoupling is not necessary at lower frequencies because the resistance at the gate of a common gate stage does not appear as a significant impedance at the source; thus a small decoupling capacitor suffices.

V. Amplifier Fabrication and Modeling

The amplifier described here was fabricated in a 1 μm GaAs MESFET process at TriQuint Semiconductor. The ion-implanted, recessed-gate depletion mode MESFET's in this technology display a nominal pinchoff voltage of −1.5 V, an f_T of 12 GHz, an $I_{DSS} = 140$ mA/mm, and a $g_m = 135$ mS/mm at $V_{GS} = 0$ V, $V_{DS} = 2.5$ V. These and other MESFET device parameters are summarized in Table I. Simulations were performed using a modified SPICE JFET model [17] supplied by TriQuint Semiconductor and further enhanced to attain agreement with



R_{fb}	575 Ω
C_{fb}	75 fF
R_{s1}	250 Ω
R_{s2}	250 Ω
V_{s1}	−2 V
V_{s2}	−1 V
V_{DD}	+5 V
V_{SS}	−5 V
M1	500 μm
M1A	200 μm
M2	150 μm
M3	200 μm
M4	70 μm
M5	100 μm
M6	100 μm
M7	100 μm
M8	250 μm
M8A	100 μm
M9	70 μm
M10	100 μm
M11	40 μm
M12	100 μm
M13	100 μm
M14	100 μm
M15	150 μm
M16	150 μm
M17	150 μm
M18	150 μm
M19	10 μm
M20	40 μm

Fig. 6. Wide-band amplifier CASC. Device sizes in inset.

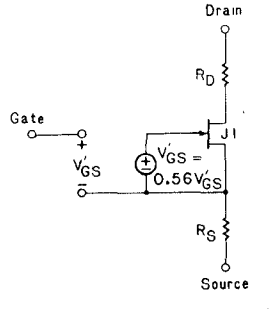
TABLE I
TYPICAL MESFET PARAMETERS

I_{DSS}	42mA
V_P	−1.5V
g_m	40mS
C_{gs}	525fF
C_{gd}	45fF
C_{ds}	75fF
R_{ds}	450Ω
f_T	12GHz

$W = 300\ \mu m$; $L = 1\ \mu m$; $V_{GS} = 0$; $V_{DS} = 2.5$.

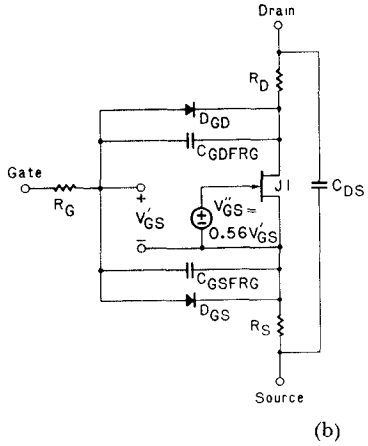
measured device performance. The dc MESFET subcircuit (Fig. 7(a)) utilizes a voltage-controlled voltage source to obtain independent control of the device pinchoff voltage, V_p, and the value of V_{ds} at which the device enters saturation. Comparison of measured and simulated dc output curves for a 300 μm MESFET (Fig. 8(a)) shows adequate agreement over all areas of operation. To predict the effects of frequency-dependent output conductance dispersion [18], a similar model was used (Fig. 7(b)) with parameters adjusted to reflect the increased output conductance at frequencies in excess of ≈10 kHz. This model also exhibits good agreement with measured data (Fig. 8(b)).

The dc model (Fig. 7(a)) was used in all simulations involving bias point calculations. The ac model (Fig. 7(b))



(a)

R_G	25 Ω
R_D	30 Ω
R_S	3.0 Ω
J1 Parameters	
Area Factor	300
V_{th}	−0.9 V
λ	10 mA/V
β	188 μA/V²
I_{sat}	≈ 0



(b)

R_G	25 Ω
R_D	30 Ω
R_S	30 Ω
C_{GSFRG}	60 fF
C_{GDFRG}	60 fF
C_{DS}	91.8 fF
D_{GS} Area Factor	600
D_{GD} Area Factor	112
Diode Parameters	
C_{jo}	1.1 fF
V_j	0.5 V
I_{sat}	1.0 fA
N	1.16
M	0.5
F_C	0.0
J1 Parameters	
Area Factor	300
V_{th}	−0.9 V
λ	125 mA/V
β	150 μA/V²
I_{sat}	≈ 0

Fig. 7. (a) dc model of 300 μm/1 μm MESFET used in SPICE simulations. (b) ac model of 300 μm/1 μm MESFET used in SPICE simulations.

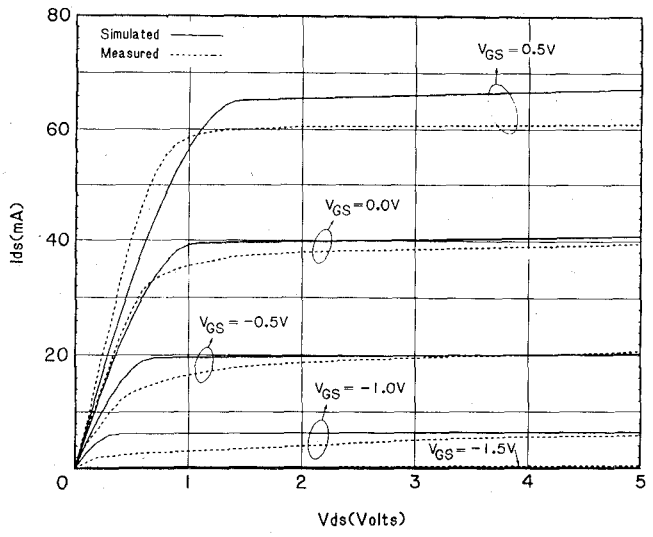


Fig. 8. Comparison between measured (dashed) and simulated (solid) $I-V$ characteristics of MESFET at (a) low frequencies and (b) high frequencies.

was then used for accurate prediction of high-frequency performance. During ac simulations, ideal current and voltage sources were added to the circuit to correct for bias point perturbations introduced by the effects of the high output conductance inherent in the ac model. This step was necessary because SPICE cannot automatically use different models for ac simulations and bias point calculations.

The bias-dependent terminal capacitances C_{gs} and C_{gd} were modeled by the junction capacitance of reversed biased diodes D_{gs} and D_{gd}, respectively. C_{ds} was modeled with a voltage-independent capacitor proportional to the device width. The junction areas of D_{gs} and D_{gd} and the size of C_{ds} were selected to obtain a good match between measured and simulated values of terminal capacitances at the nominal bias point $V_{GS}=0$ V, $V_{DS}=2.5$ V. These elements were then scaled proportionally with device width. A major weakness of the above method is that the models

TABLE II
SUMMARY OF AMPLIFIER PERFORMANCE

Gain	26dB
Bandwidth	3.2GHz
Worst Input VSWR	2.5:1
Worst Output VSWR	2.5:1
Noise Figure	8dB
P_{-1dB}	8dBm
Saturation Power	10dBm
Power Dissipation	850mW
Die Size	1mm×1mm
Active Area	.42mm^2

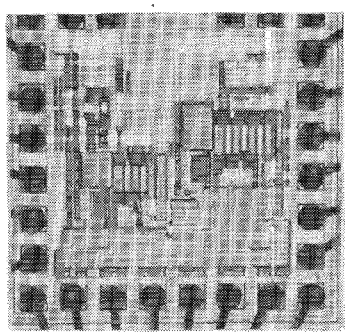


Fig. 9. Photograph of wide-band amplifier wire-bonded in microwave package.

yield erroneous values of capacitance for bias points far away from the nominal. This lack of accuracy in modeling the nonlinear voltage-dependent capacitances of MESFET's was another motivation for developing the circuit technique described above, which allows external adjustment of the amplifier frequency response.

VI. Amplifier Performance

The results of this study in terms of gain, bandwidth, and power dissipation are summarized in Table II. The amplifier chip (Fig. 9) was fabricated as part of a multiproject chip reticle. The chip size was fixed (1.15 mm×1.15 mm) and the bond-wire pad pattern was standard (100 μm square pads on 150 μm centers). The active area of the amplifier is 600 μm×700 μm, giving a total active chip area of 0.42 mm^2. The diced chips were mounted in a microwave package and bonded using 1 mil diameter bond wires approximately 15 mils in length. This package was then mounted on a specially designed microstrip test fixture. All testing was performed on *packaged* parts using this test fixture—no high-frequency wafer probes were used. The measured insertion gain of the amplifier indicates a dc gain of 26 dB and a −3dB bandwidth of 3.2 GHz, in good agreement with the simulated response (Fig. 10). The simulation above includes the effects of 0.75 nH bond-wire inductances. The input and output VSWR (Fig. 11) are better than 2.5:1 over the passband. The measured

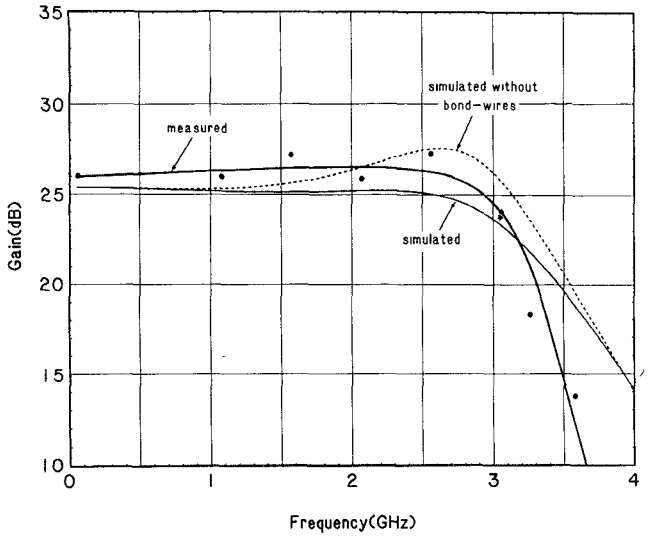


Fig. 10. Measured (●) and simulated (solid) frequency responses of amplifier. Simulation with zero bond-wire inductance (dashed) also included.

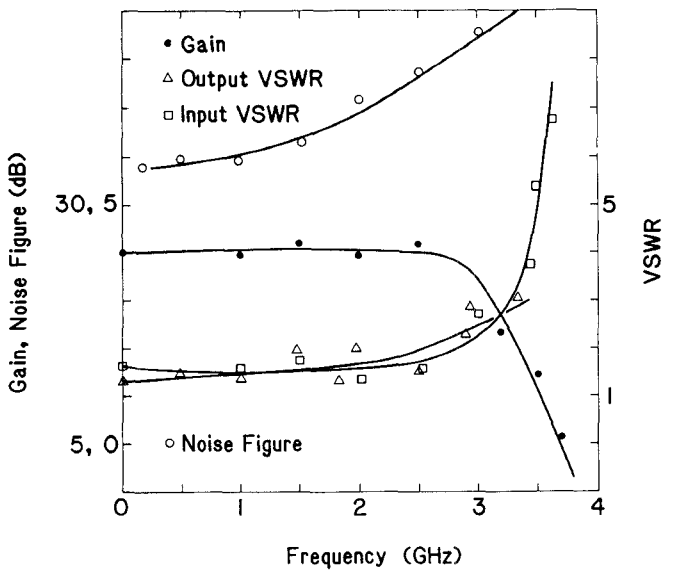


Fig. 11. Measured frequency response, input and output VSWR, and noise figure.

noise figure (Fig. 11) remains at or below 6 dB from midband to 1 GHz and degrades to 8 dB at the band edge. It is worth noting that no effort was made to minimize the noise figure during design of the circuit. The amplifier exhibits a saturated output power of 10 dBm, and an output power of 8 dBm at the −1 dB gain compression point. Nominal dc power dissipation for the circuit is 850 mW when operating with standard +5 V and −5 V supplies; however, V_{ss} can be reduced to −3 V without affecting the amplifier performance, thereby reducing the power dissipation to 750 mW.

The action of the stability network was determined by measuring the frequency response for various values of the dc control voltages $V_{\text{adjust 1}}$ and $V_{\text{adjust 2}}$ (Fig. 12). These curves show that excessive peaking and instability can be controlled by the proposed method.

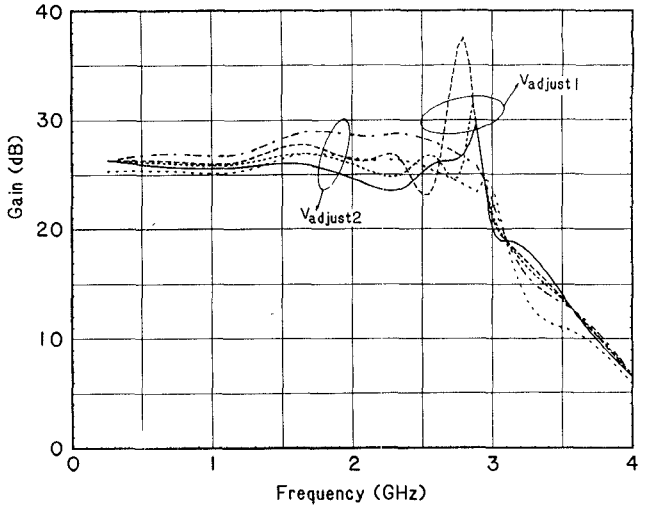


Fig. 12. Measured peaking response for various $R-C$ time constants in the cascode feedback paths.

VII. Comparisons with Previous Work

Several GaAs MESFET high-frequency amplifiers using cascode building blocks have been reported previously [10], [19], [16], [20], [21]. None of these topologies have utilized a cascode stage within a feedback loop. Cascode feedback amplifiers have been designed in a 0.5 μm NMOS process [22] for operation in the hundreds of megahertz range; however, stable operation of such an NMOS cascode circuit was limited to well below 1 GHz. While external adjustment of amplifier frequency response has been investigated for bipolar broad-band amplifiers [23]–[25], no such techniques have been reported for GaAs high-frequency amplifiers until now.

A summary of several recently reported GaAs MESFET wide-band amplifiers (Table III) allows comparison of the present work with previous topologies. Care should be taken when referring to this summary since comparing amplifiers with different design requirements and applications can be misleading. Only GaAs amplifiers without lossless input matching elements are included, although some of the entries describe amplifiers which use interstage inductors or transmission lines. Table III lists the midband gain, −3 dB bandwidth, maximum input and output VSWR over the specified bandwidth, maximum noise figure over the range from midband to the −3 dB frequency, input topology, gate length, chip area, and power dissipation for each entry. All designs but two use the common source input topology. Several of the amplifiers described utilize an open-drain output stage [9], [6], [4]. Since this type of circuit exhibits high output impedance, the amplifiers will display poor output VSWR. To obtain a more meaningful comparison to an *output matched* amplifier, the gain of these circuits has been derated by 4 dB. This is the approximate reduction in gain which would result if the amplifiers were reverse terminated with a 50 Ω resistive load to achieve a good output match. The corresponding output VSWR has been listed simply as "low" to indicate that although the amplifiers have not been tested in this

TABLE III
COMPARISON OF GaAs WIDE-BAND MONOLITHIC AMPLIFIERS

Reference	Gain (dB)	Bandwidth (MHz)	Input VSWR	Output VSWR	Noise Figure (dB)	Area (mm^2)	Input Topology	Gate Length (μm)	Power (mW)
This Work (UCLA)	26	DC-3200	<2.5	<2.5	8.5	1.3*	CS	1.0	750
Estreich[9] (HP)	22†	5-3300	<1.3	low	9.0	0.27	CG	1.0	?
Honjo[26] (NEC)	13.5	DC-2800	>2.5	<1.6	7.0	1.1	CS	1.2	?
Honjo[27] (NEC)	16	9-3900	<2.5	<3.1	3.0	0.96	CS	1.0	170
Hori[28] (Toshiba)	27	DC-1200	<7.0	<1.4	2.0	2.25	CS	1.0	1000
Imai[5] (NTT)	22	DC-2500	<1.9	?	7.0	0.96	CS	0.7	?
Imai[6] (NTT)	5.6†	DC-4000	<2.1	low	8.0	0.56	CS	1.0	?
Imai[4] (NTT)	10†	DC-3000	<1.7	low	6.0	0.64	CS	0.7	500
	18†	DC-2700	<1.7	low	7.0	0.96	CS	0.7	960
Manz[8] (Anadigics)	22	DC-2500	<1.5	<2.5	5.5	?	?	1.0	830
Nishiuma[14] (Matsushita)	28	30-1700	<3.0	<3.0	2.2	0.83	CS	?	200
Onoda[29] (NEC)	14	50-3800	<1.9	<1.2	5.0	1.3	CS	?	330
Pauker[30] (LEPA)	20	200-3000	<1.5	<2.0	?	?	CG	0.8	?
Petersen[31] (Rockwell)	12	DC-2000	<2.6	<1.7	3.0	2.2	CS	1.0	210
Tajima[32] (NTT)	15	200-2000	<1.9	<1.4	?	1.4	CS	1.0	120
Weitzel[33] (Motorola)	25	100-1500	<4.0	<4.0	7.0	1.0	CS	1.0	?

*Total area of the multiproject chip is 1.3 mm^2. Active chip area is 0.42 mm^2.
†Published gain has been derated by 4 dB to obtain 50 Ω match at output port.

configuration, the output VSWR should, in principle, be low.

Although not stated explicitly, several of the references in Table III used high-speed wafer probes to obtain test data. This evaluation method minimizes packaging parasitics, such as bond-wire inductances, which can significantly degrade the high-frequency performance of the amplifier. The data for this amplifier were obtained from packaged parts that included all test fixture parasitics. The frequency response of the new cascode feedback amplifier was simulated with bond-wire inductances removed (Fig. 10), indicating that the amplifier bandwidth would improve from 3.2 GHz to 3.4 GHz.

VIII. CONCLUSIONS

Feedback around cascode building blocks has been shown to be a powerful means of enhancing the gain and bandwidth of broad-band microwave amplifiers. To our knowledge, the gain–bandwidth product of this amplifier exceeds that of any other such matched wide-band amplifier fabricated in a 1 μm MESFET technology. The cascode implementation displays comparable noise figure, VSWR, and output power to existing amplifiers as well. A novel adjustment method to ensure circuit stability while maximizing frequency response has been described along with a simple method for biasing the common gate transistors of the cascode circuit.

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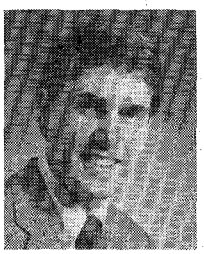

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